

REMARKS/ARGUMENTS

Favorable reconsideration of this application as presently amended and in light of the following discussion is respectfully requested.

Claims 1-10 and 14-17 are pending in the present application. Claims 11-13 have been canceled, claims 1, 6 and 10 have been amended and claims 16 and 17 have been added by the present amendment.

In the outstanding Office Action, the abstract was objected to; and claims 1-15 were rejected under 35 U.S.C. § 102(e) as anticipated by Bartholomay et al.

The abstract has been amended in light of the comments noted in the Office Action. Accordingly, it is respectfully requested this objection be withdrawn.

Claims 1-15 stand rejected under 35 U.S.C. § 102(e) as anticipated by Bartholomay et al. This rejection is respectfully traversed.

Amended claim 1 is directed to an inter-processor communication apparatus of a mobile communication system including a data-FIFO configured to be directly coupled to a transmission bus and configured to store a receiving data from a master, and a slave-logic configured to control a writing operation of the receiving data for the data-FIFO and count a length of the receiving data until an end-tap signal is inputted. Also included is a length-FIFO directly connected to the slave-logic and configured to store the data length counted by the slave-logic, and a CPU separately connected to the slave-logic, the data-FIFO and the

length-FIFO and configured to continuously read the data stored in the data-FIFO as much as the data read from the length-FIFO when an interrupt signal is inputted from the slave-logic. Independent claims 6 and 10 include similar features in a varying scope.

In a non-limiting example, Figure 2 illustrates an inter-processor communication apparatus of a mobile communication system including a data-FIFO 100 configured to be directly coupled to a transmission bus Tx Bus and configured to store a receiving data from a master, a slave-logic 104 configured to control a writing operation of the receiving data for the data-FIFO 100 and count a length of the receiving data until an end-tap signal is inputted, a length-FIFO 106 directly connected to the slave-logic 104 and configured to store the data length counted by the slave-logic 104, and a CPU 102 separately connected to the slave-logic 104, the data-FIFO 100 and the length-FIFO 106 and configured to continuously read the data stored in the data-FIFO 100 as much as the data read from the length-FIFO 106 when an interrupt signal is inputted from the slave-logic 100.

Thus, according to the present invention, the inter-processor communication apparatus has a simplified construction including the claimed length-FIFO, the CPU, the data-FIFO and the slave-logic. That is, as shown in Figure 2, for example, the apparatus includes a simple structure, which reduces the cost of the apparatus and allows for simplified repairs. For example, the CPU 102 in Figure 2 can be easily be replaced without having to

also replace the slave-logic 104 or other items, because the CPU 102 is separately connected to the other components.

On the contrary, as shown in Figure 1 of Bartholomay et al., the apparatus is extremely complex and does not include a CPU that is separately connected to a slave-logic, a data-FIFO and a length-FIFO as in the present invention. Note the Office Action indicates the host controller corresponds to the claimed slave-logic and CPU, the message length register 16 corresponds to the claimed length-FIFO, and the FIFO 12 corresponds to the claimed data-FIFO. However, comparing the structure shown in Figure 2 of the present invention with the structure shown in Figure 1 of Bartholomay et al., it can be seen that the device of Figure 2 of the present invention is greatly simplified.

Further, as shown in Figure 1 of Bartholomay et al., the FIFO 12 is not configured to be directly connected to the transmission line 22. Rather, another element HDLC 20 is disposed therebetween. The HDLC 20 is a high level data link control equipment that monitors the down link channel, strips opening and closing flags for messages, removes stuffed zeros, and generally reconstitutes the original message (see column 4, lines 23-27). Thus, the device shown in Figure 1 of Bartholomay et al. is significantly more complex than the claimed invention. Further, as noted above, Bartholomay et al. does not teach or suggest a CPU separately connected to the length FIFO, the slave-logic and the data-FIFO. Thus, the advantageous of the present invention are not achieved with Bartholomay et al.

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Accordingly, it is respectfully submitted independent claims 1, 6 and 10 and each of the claims depending therefrom are allowable.

In addition, new claims 16 and 17 have been added to set forth the invention in a varying scope, and Applicant submits the new claims are supported by the originally filed specification. In particular, the claims are supported at least by the specification at page 6, line 2-17. New claim 16 depends on claim 1, and further recites a communication between the claimed elements. Dependent claim 17 is similar to dependent claim 16, but depends on claim 10. It is respectfully submitted new claims 16 and 17 further define over Bartholomay et al.

CONCLUSION

In view of the foregoing amendments and remarks, it is respectfully submitted that the application is in condition for allowance. If the Examiner believes that any additional changes would place the application in better condition for allowance, the Examiner is invited to contact the undersigned attorney, **David A. Bilodeau**, at the telephone number listed below.

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To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this, concurrent and future replies, including extension of time fees, to Deposit Account 16-0607 and please credit any excess fees to such deposit account.

Respectfully submitted,
FLESHNER & KIM, LLP



Daniel Y.J. Kim
Registration No. 36,186
David A. Bilodeau
Registration No. 42,325

P.O. Box 221200
Chantilly, Virginia 20153-1200
(703) 766-3701 DYK/DAB:cre:lew
Date: December 14, 2004

Please direct all correspondence to Customer Number 34610